ATCA Carrier Board and AMC Modules for LLRF System

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Agenda

- LLRF Control System of XFEL
- ATCA Carrier Board for XFEL
- AMC modules
- Plans for the Future
Requirements for LLRF System

- The LLRF system of XFEL accelerator will consists of ~25 distributed RF stations, each supervising 32 cavities,
- Simultaneous acquisition of data from more than 100 fast ADC channels with resolution better than 14 bits and sampling rate 100 MHz,
- Real-time data processing (in range of hundreds of nanoseconds),
- Processing power for more complex algorithm (diagnostics, monitoring and exceptions),
- Collecting and processing data from piezo drivers and sensors,
- Modularity and upgradeability,
- Hot-plug and easily cabling,
- High availability and reliability.
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ATCA (Advanced Telecommunication Computing Architecture) standard can fulfil most of the requirements of the LLRF control system for XFEL.
ATCA-based LLRF system

The proposed architecture of LLRF system requires:

- Dedicated ATCA carrier board for AMC modules with RF signals distribution,

- A number of AMC modules with various functionalities:
  - DAQ module with eight ADCs (TEWS TAMC 900),
  - Vector Modulator module,
  - Timing module,
  - AMC module with digital and analogue I/Os,
  - DAQ module with high-speed ADCs,
  - Radiation monitoring module (RadMon),

- Piezo-controller for Lorentz force detuning designed according to ATCA standard,
- DAQ module for RF Direct Sampling (AMC/ATCA).
Architecture of LLRF System

[Diagram showing the architecture of the LLRF system with various components and connections, including ADCs, FPGAs, PCIe switches, Root Complex, Piezo Compensator, and Shelf Manager.]
ATCA Carrier Board – Requirements (1)

- **Processing power**
  - Real-time algorithms (Xilinx Virtex 5 FPGA XC5VLX50T),
  - Complex algorithms (TigerSHARC DSP TS201, 600 MHz),

- **Analogue signals**
  - 24 differential signals (probe, forward and reflected power),
  - Main RF frequency input/output (f=1.3 GHz),

- **Digital communication interfaces**
  - PCIe / Gb Ethernet,
  - Low latency links for LLRF controller feedback,
    - LVDS,
    - Xilinx Rocket IO,

- **Power supply**
  - Main DC/DC converter for Management and Payload Power Supply
  - Local power supply (FPGAs, DSP, memories,...)
ATCA Carrier Board – Requirements (2)

- Hardware management
  - IPMC (power supply, hardware diagnostics),
  - AMC modules supervision,
  - Critical parameters monitoring (temperature, voltages, clocks, ...),

- Timing and clock distribution
  - 3 trigger signals (LVDS levels),
  - 2-3 clock signals (LVDS levels from AMC-based timing module),

- Support three AMC modules,
  - Deliver power supply,
  - Supply all analogue and digital signals via AMC connector,
  - Module diagnostics and monitoring,
  - Hot-plug support,
  - Firmware upgrade.
ATCA Carrier Board for LLRF System

Main power supply
Main processing power

Analogue RF Signals F=1.3 GHz

PCIe extermal connector

AMC modules bays

RTM module

RF signals

AMC quad-row connector
Some of AMC modules need similar functionalities, e.g. processing power, communication interface, Module Management (MMC).
AMC_B - AMC Carrier Module (2)

Bottom module with main functionality

Top module with control logic
Photograph of AMC_B carrier module

- All subsystems of the module were successfully debugged and tested,
- FPGA processing power, memory, power supply, MMC, interfaces (PCIe, LLL, debug interface), SystemACE.
Timing Module

- Generate frequencies and triggers required by LLRF system from frequency provided by Master Oscillator:
  - Clock frequencies: 10 MHz – 100 MHz,
  - Clock stability better than 5 ps, (desirable < 2 ps),
  - Receive and decode timing signals from the existing FLASH timing (optical fibre input).
Vector Modulator Module

- Modulates LO frequency according to I and Q signal provided by LLRF controller:
  - LO input frequency: 1.3 GHz,
  - Nominal Input level: $\pm 1 \text{ V}_{pp}$,
  - Nominal Input power range: $\pm 6 \text{ dBm}$,
  - Output frequency: 1.3 GHz.
DAQ Module for RF Direct Sampling (1)

- Module dedicated for direct sampling of cavity probe signals.

- Requirements:
  - Eight analogue channels dedicated for direct sampling,
  - High-frequency ADCs (12-bit, 1000 MSPS ADC, 2.1 GHz Input Bandwidth, e.g. TI ADS5400),
  - FPGA processing power,
  - Clock and Trigger distribution,
  - Module Management Controller,
  - Power supply.
Initially planned as AMC module, currently developed as full-size ATCA board (space and power limitations),

Development in progress.
- Management of ATCA carrier board,
- Management of AMC modules,
- Monitoring of ATCA health (diagnostics),
- E-Keying for PCIe, Gb Ethernet and user defined Low Latency Connection,
- Monitoring of temperature, power supply, clocks, etc...
Intelligent Platform Management Controller (3)

IPMI bus

IPMC

MMC
Tests of the ATCA-based LLRF system

- The ATCA carrier board and AMC modules were tested during FLASH test in August/September 2009 (FLASH accelerator at DESY),

- The basic functionality was demonstrated but the system requires further improvements,

- Currently we are working on the second revision of ATCA carrier board and AMC modules.
## Milestones

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<tr>
<th>Milestone Description/title</th>
<th>Delivery Month</th>
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<td>10.6.1. Design and manufacturing of the carrier board prototypes</td>
<td>M18</td>
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<tr>
<td>10.6.2 Design and manufacturing of the AMC modules with fast analogue and digital IO</td>
<td>M24</td>
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<tr>
<td>10.6.3 Design and manufacturing of the AMC board with ultra fast ADC</td>
<td>M24</td>
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<tr>
<td>10.6.4 Design and manufacturing of AMC radiation dosimeter</td>
<td>M18</td>
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<td>10.6.5 Report on tests and calibration of the radiation dosimeter</td>
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<tr>
<td>10.6.6 Designed and manufactured Frequency Synthesizer Board (AMC)</td>
<td>M24</td>
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<tr>
<td>10.6.9 Design and fabrication of AMC, modules for controlling step motors, piezo and waveguide tuners</td>
<td>M24</td>
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Publications


Plans for the Future

- Design of the second version of carrier board
  - “Tune” the total cost of single RF station,
  - Only Gb Ethernet used as a main communication interface, no PCIe,
  - IPMC controller with 10/100 Mb Ethernet,
  - FPGA/DSP firmware/software upgrade via IPMI interface (HPM.1) or Gb Ethernet,
  - Improved clock and signal distribution,
  - Finish and debug ATCA-based piezo controller.
Thank you for your attention